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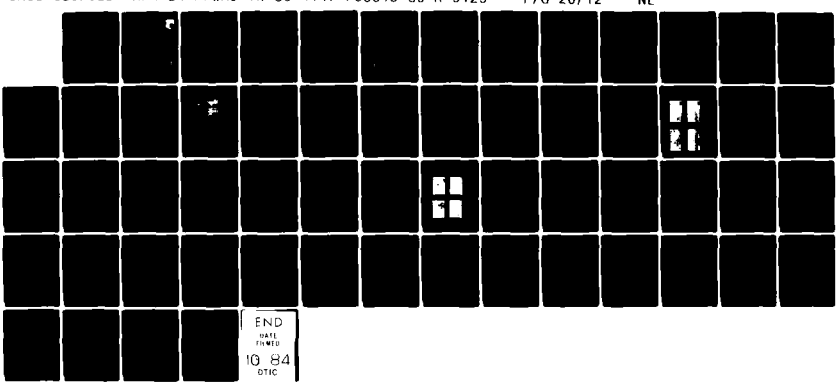

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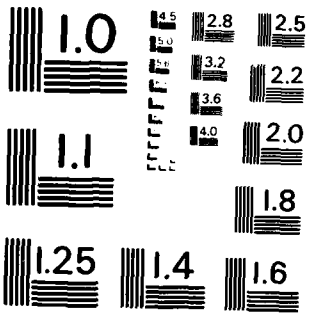

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CURRENT CONTROLLED LPE GROWTH OF SEMICONDUCTORS

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The primary objective of this study was to determine the optimum growth parameters for preparing uniform epitaxial crystalline layers of InAs, InSb, InAsSb and Si using the current controlled liquid phase epitaxy (CCLPE) technique. The original objective was later altered and the effort concentrated on the growth of InAs and Si by CCLPE.

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20. p-type (Zn-doped) and n-type (Ge-doped) layers of InAs were grown by CCLPE on undoped InAs substrates at a constant furnace temperature in the temperature range of 570 - 670°C. The growth materials were characterized by their surface morphology and epilayer thickness. Hall measurements were performed on the grown layers in the temperature range of 10 - 300K to determine the dependence of mobility and carrier concentration on temperature. The dependence of the I-V characteristics of p-n InAs on temperature was also investigated. InAs epilayers were also grown by LPE over the same temperature range. From the LPE growth rate versus temperature results, the diffusion coefficient of As in In was calculated to be $D = 525\exp\left(-\frac{1.4 \times 10^4}{T}\right)$ cm^2/sec with an activation energy for diffusion of 1.2eV (27.5Kcal/mole). CCLPE growth results indicated a linear relationship between the growth rate of InAs and current density. The differential mobility of As in In was computed as $\mu = 0.008 cm^2/V\text{-}sec$ at 620°C.

CCLPE growth of Si was also attempted using either an In or a Ga melt in the temperature range of 850 - 1050°C. Almost all of the growth experiments were unsuccessful primarily because of the formation of a stable oxide layer on the silicon substrate surface and/or silicon source material in the melt. Most of the efforts were subsequently directed towards elimination or reduction of the oxide layer. The best experiments yielded only spotty growths. On the basis of the results it was decided that a more sophisticated system utilizing a controlled mixture of HF or HI might be necessary to eliminate the oxide problem. However, because of insufficient remaining time and funds, and questions about possible reaction of the new environment with the quartz tube and its effect on impurity concentration, this approach was not pursued.

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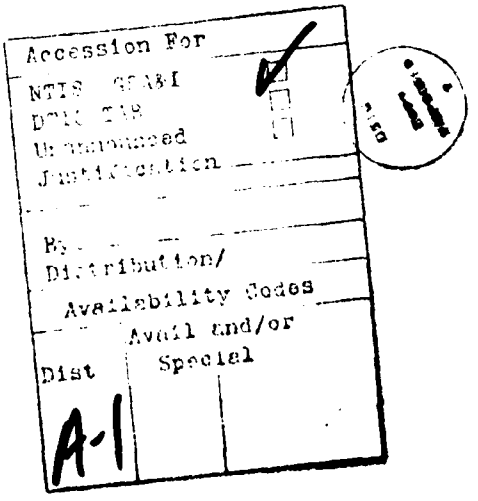


SECTION I

INTRODUCTION

Epitaxial materials have been used extensively in the fabrication of opto-electronic devices and integrated circuits. Specific material requirements for high performance devices mandate a detailed understanding of the material properties affected by the epitaxial growth process, especially the physical parameters relating to device performance.

Liquid phase epitaxy (LPE) has been used in applications requiring high purity layers and abrupt junctions from low temperature depositions. Improvements in the control of crystal quality of liquid phase epitaxial layers have been made by the use of the current controlled LPE (CCLPE) growth technique.

Current controlled growth is obtained when an electric current is applied across the melt-substrate interface in a LPE system. This growth technique is carried out in a modified LPE growth system and takes place at constant furnace temperature. CCLPE was first applied to the InSb system[1] and more recently to other III-V compounds such as GaAs[2-4], InP[5], GaAℓAs[6] and InGaAs[7]. The results have shown that CCLPE yields high quality epitaxial layers exhibiting excellent surface morphology and thickness uniformity, high electron mobilities, and fairly constant impurity profiles.

The primary objective of this study was to determine the optimum growth parameters for preparing uniform epitaxial crystalline layers of InAs, In Sb, InAsSb and Si using the CCLPE technique. The original objectives was later altered and the effort concentrated on the growth of InAs and Si by CCLPE. The material characterization included: surface morphology and layer uniformity, carrier concentration and mobility determination. Ga and In melts were used for the low temperature growth of silicon.

SECTION II

2.0 GROWTH OF InAs

InAs and InSb are materials of considerable potential for the fabrication of infrared emitters and detectors which operate in the wavelength range of 3.5 - 7.3μm. For practical applications, thin films of InAs and InSb are used as Hall generators and magnetoresistive elements. InAs and InSb are worth considering because of the high electron mobility.[8]

In this work, p-type (Zn-doped) and n-type (Ge-doped) layers of InAs were grown on undoped InAs by CCLPE at a constant furnace temperature of 620°C. Detailed results are presented in Appendices A and B. A summaried description of this study is given below.

2.1 Experimental Apparatus and Procedure

Figure 1 is a schematic diagram of the experimental apparatus used in the LPE and CCLPE growth of InAs on InAs substrates. Three Eurotherm temperature controllers were used to control the furnace temperature. A schematic cross section of the horizontal boat assembly used for the growth of InAs is shown in Fig. 2. The body of the boat was made from two high purity graphite parts with the bottom part electrically insulated from the top part as shown in Fig. 3.

Two InAs melts were placed in the second and fourth well of the top part of the boat. The melts consisted of a 6N grade indium and an appropriate amount of InAs. The dummy melt consisted of 6N pure In and sufficient amount of InAs to keep the melt initially undersaturated. Both the InAs melts and the dummy melt were baked at 700°C for 24 hours and subsequently an InAs substrate was mounted at the end of the graphite plunger in order to (1) insure the saturation

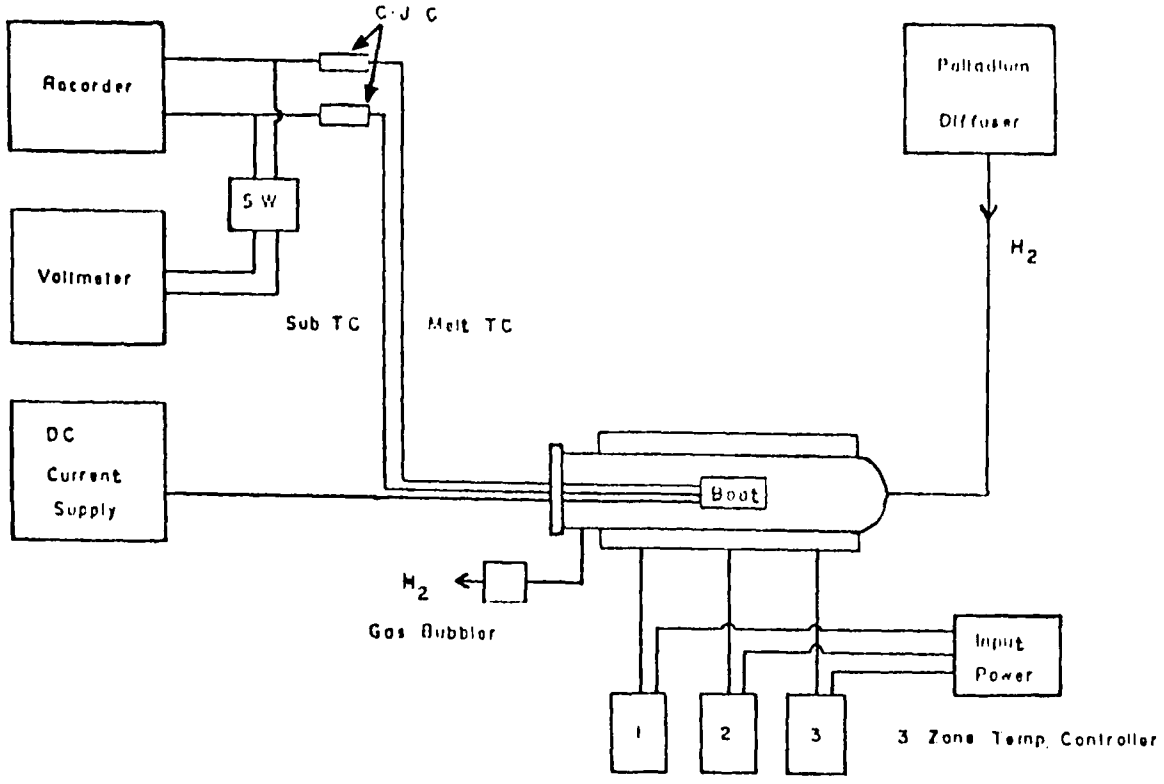


Figure 1. A block diagram of the CCLPE system used to grow indium arsenide.

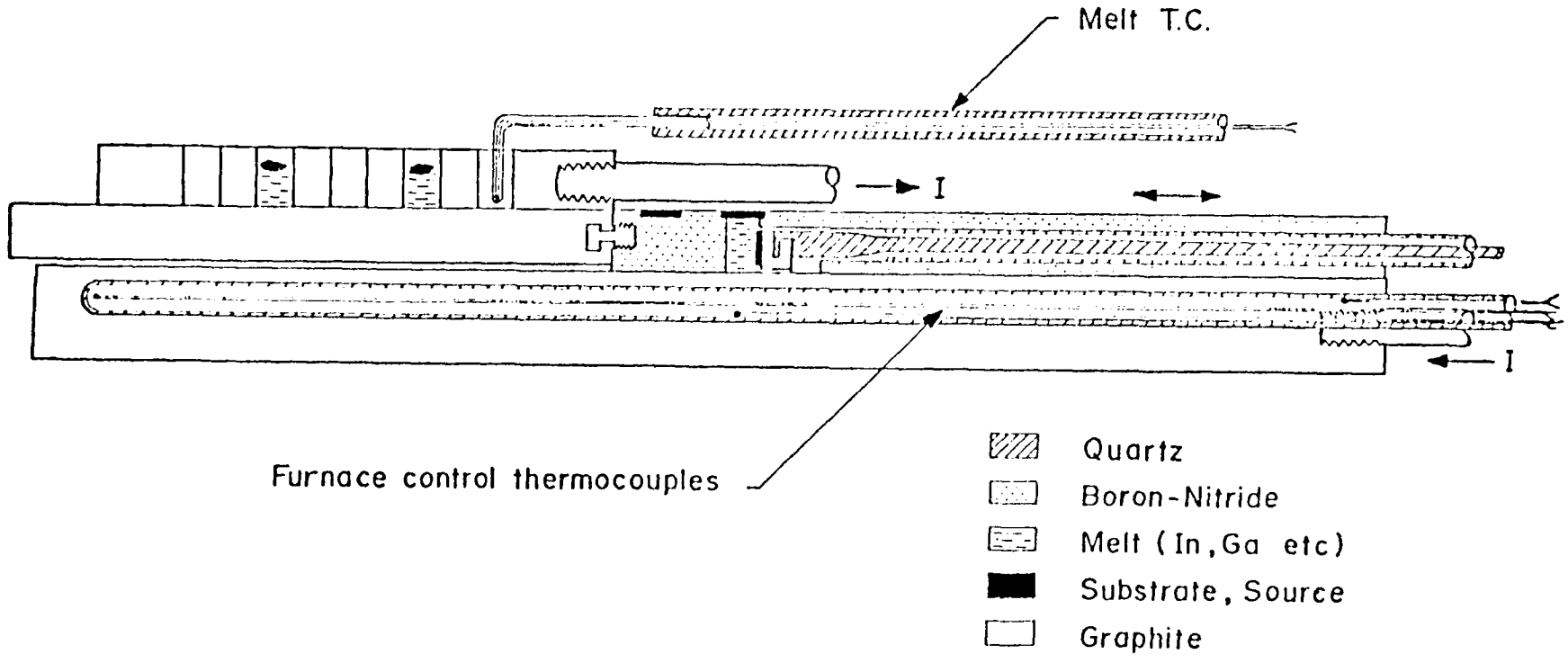


Figure 2. A Schematic cross section of the horizontal boat assembly used for CCLPE.

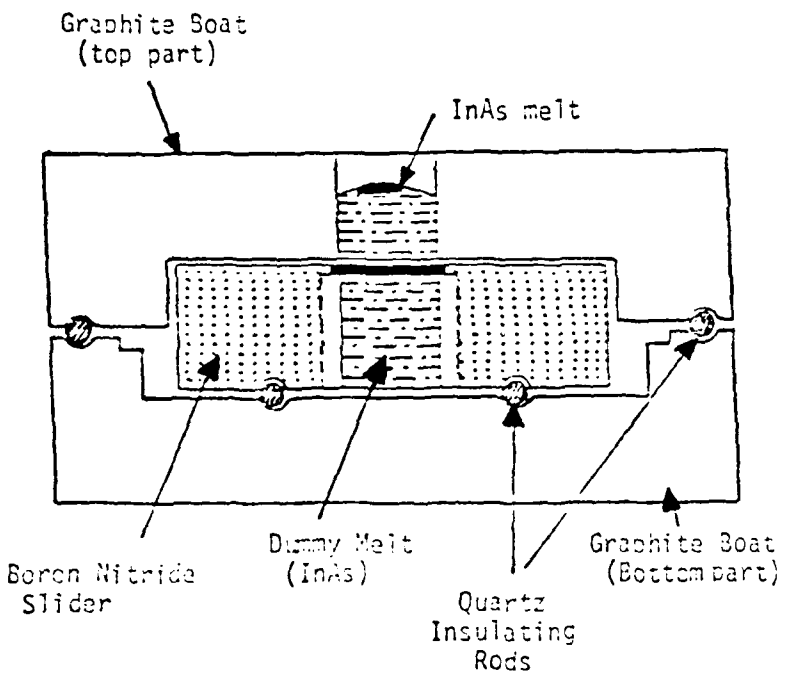


Figure 3. A cross-section of the boat with the melt in contact with the substrate.

of the dummy melt, and (2) enhance melt retraction as the plunger is pulled back after the growth is terminated.

After careful preparation of the InAs substrate and melts (see Appendix A), the substrate with mirror polished surfaces on both sides was loaded into the boat. The furnace was then turned on and allowed to stabilize at a temperature of 620°C. After approximately seven hours equilibriation time, the substrate was slid slowly beneath the first InAs melt and after a 10 second equilibration with the melt, the current was turned on while simultaneously advancing the dummy melt underneath the substrate to make electrical contact to the back surface.

Current densities of 2.5 to 15 A/cm^2 were used for periods of 15 to 60 minutes. For the growth of two layers with CCLPE, the current is turned off after the first layer is grown and the substrate is advanced beneath the second melt. The current is then turned on to grow the second layer. To terminate the growth, the current is turned off and the slider is pulled back while the dummy melt is retracted to break contact with the back surface of the substrate.

2.2 Experimental Results and Discussion

During this study of Current Controlled growth of InAs on (100) oriented InAs substrates, the effect of prolonged baking (about 7 hours) of the subsbrate, prior to growth, on the quality of the substrate and substrate surface was investigated. Hall measurements were initially performed on baked and unbaked (fresh) samples to determine the effect of baking on the substrate electrical characteristics.

The grown materials were also characterized by their surface morphology and epilayer thickness. Hall measurements were performed on grown layers in the temperature range of 10 - 300K to determine the dependence of mobility and carrier concentration on temperature. The dependence of the I-V characteristics of p-n InAs on temperature was also investigated.

2.2.1 Effect of heat treatment of the substrate

To study the effect of heat treatment on the substrate during the baking of the melt, three samples were baked at 600, 620 and 640°C for a period of 7 hours each. In each of the three experiments a sample with mirror-like surface was thoroughly cleaned and etched with 1% Br_2-methanol before it was loaded into the reaction tube (the same procedure was used in the growth experiments). Subsequently, the sample was heated with the surface exposed to a purified hydrogen environment. After heat treatment, the sample was removed from the reaction tube and studied under a phase contrast microscope to determine the effect of heat on the surface morphology. The baked samples exhibited surfaces with thermal pitting and small In dots as a result of InAs dissociation. The thermal dissociation of InAs was not limited only to the surface layer but propagated upon to 10μm into the bulk of the substrate, making the substrate unsuitable for CCLPE growths.

To study the effect of baking on the electrical characteristics of the baked samples, Hall measurements on these samples and on one unbaked sample were performed in the temperature range of 10 - 300K. The results of Hall mobility versus temperature are shown in Fig. 4. An analysis of the results shows that the mobility of the baked samples decreased slightly as compared to that of the unbaked sample, and in general the behavior of the mobility versus temperature curve for the different samples as well as for the CCLPE grown materials (one and two layers) is about the same with the mobility peaks for the different samples occurring in the temperature range of 77 - 90K. The noticeable decrease in mobility in the baked samples can be attributed to an increase in defect scattering as a result of some increase in nonstochiometry in the material, which may be caused by the out-diffusion of As and/or In.

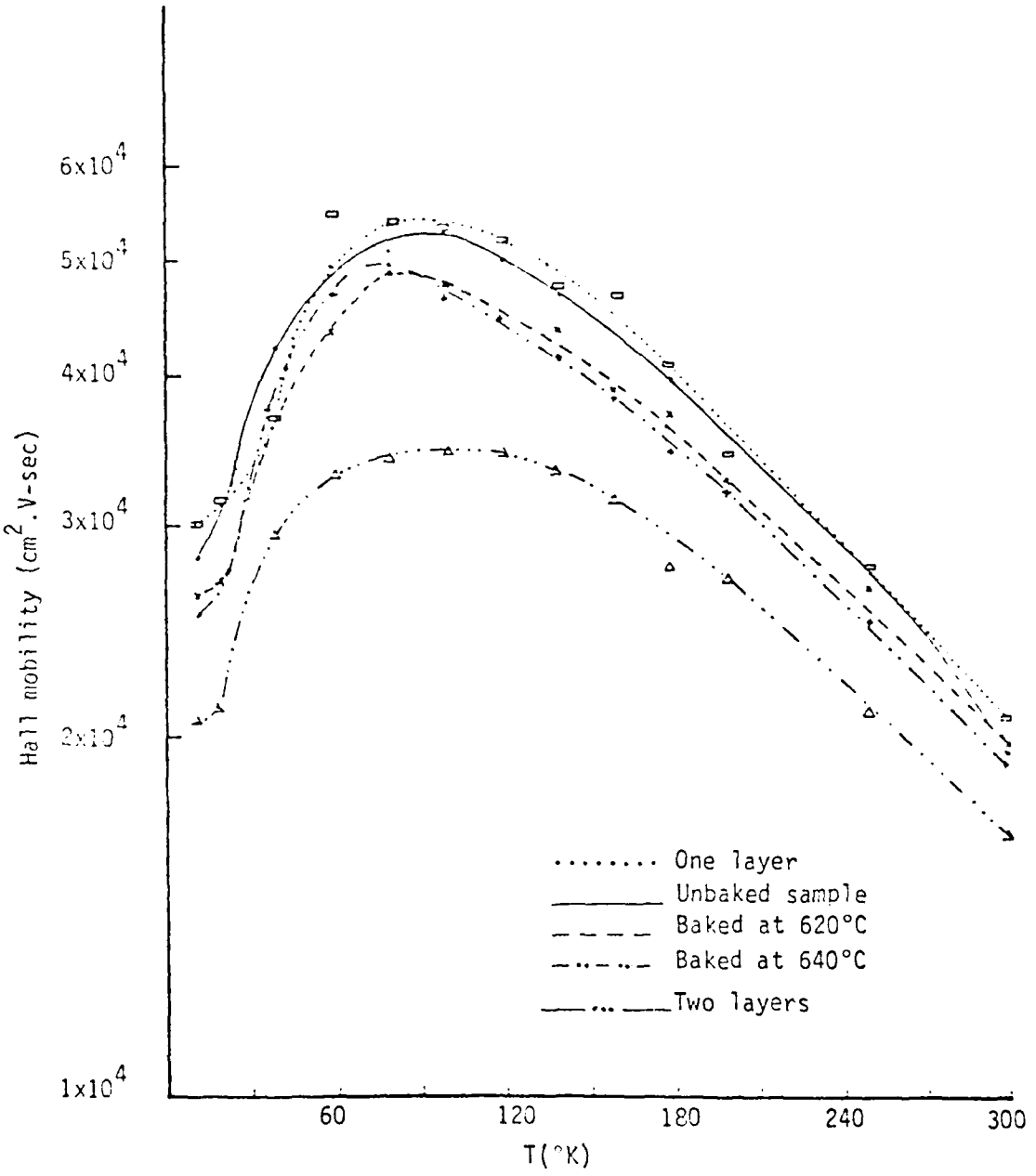


Figure 4. Hall mobility versus temperature for epitaxially grown, baked bulk-samples and unbaked (fresh) InAs samples.

The dependence of carrier concentration on temperature in two of the baked samples and one unbaked sample is shown in Fig. 5. In general the behavior is similar to that for Si over the temperature range of 60 -300K. Below 60K, the carrier concentration shows slight increases as the temperature is lowered. Such behavior is probably due to ionization of impurity states as the fermi level passes through these states.[9]

2.2.2 CCLPE Growth of InAs

Direct electric current of 5.0 A/cm^2 to 15.0 A/cm^2 was applied across the substrate melt interface, while the temperature of the furnace was kept constant at 620°C. After growth the sample was cleaved and stained in order to see the epilayer and determine its thickness. The thickness of the epilayer was determined using a calibrated scale. Figure 6 shows the surface morphology annd cleaved section of a double CCLPE layer grown with 10 A/cm^2 and 13.3 A/cm^2 each for a period of 15 minutes. A third layer is also shown in Fig. 6 which was probably caused by an out-diffusion/dissociation of the substrate. Etch pits can be seen on the epilayer surface. This pitting was the result of thermal etch with the associated loss of As and/or In. Similar results were obtained in the growth of consecutive p-type (Zn-doped) and undoped (n-type) layers as shown in Fig. 7.

Figure 8 shows a plot of the average growth velocity versus current density for InAs grown on a (100) InAs substrate by CCLPE. The results are approximated by a straight line. The linear relationship between growth velocity and current density has been verified for other binary III-V compounds. An analytical expression developed for binary systems under growth conditions dominated by electromigration is given by [10]

$$V = \mu E(C_\ell/C_s - C_\ell)) \qquad (1)$$

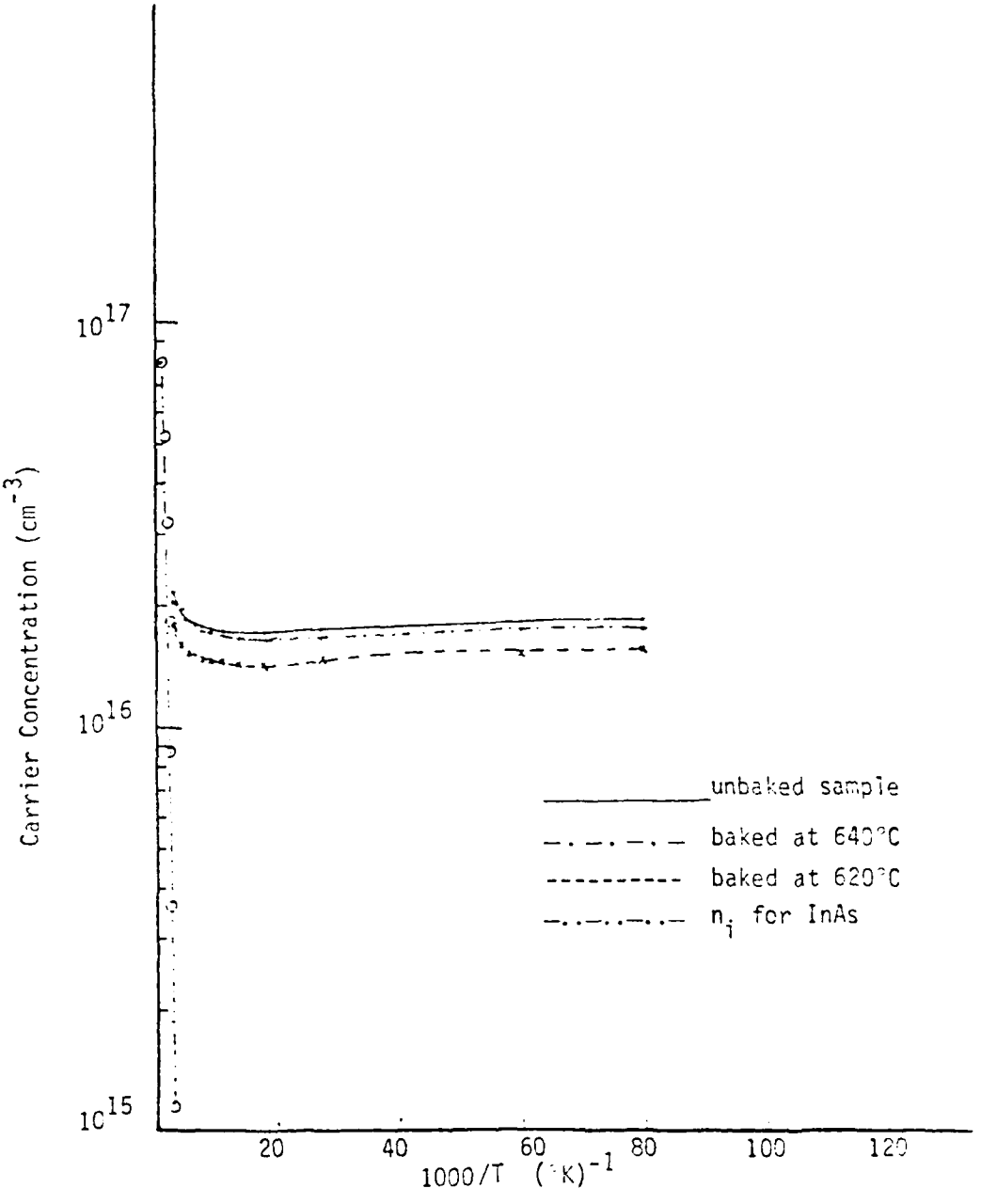
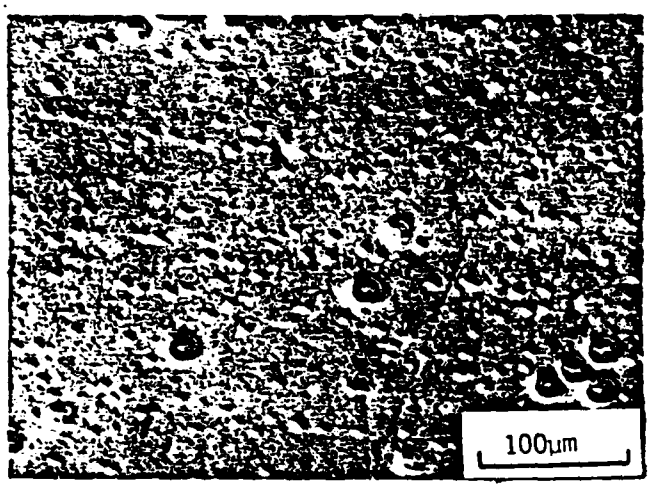
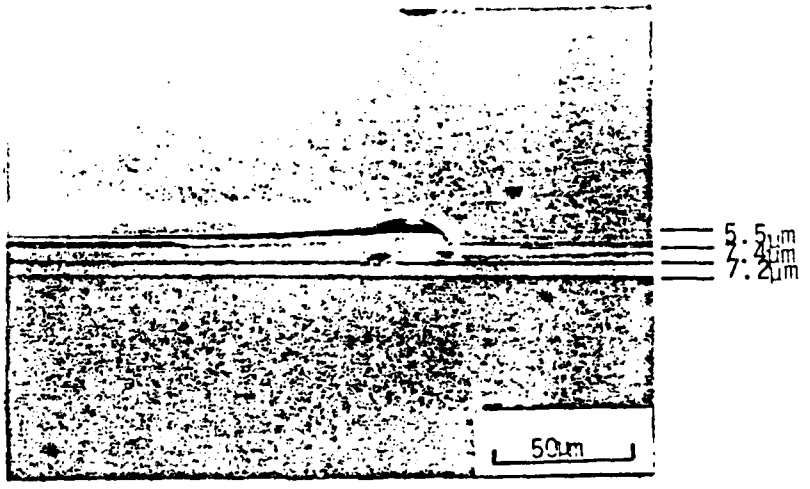


Figure 5. Carrier Concentration versus Inverse temperature for an unbaked (fresh) and two baked bulk-InAs samples.

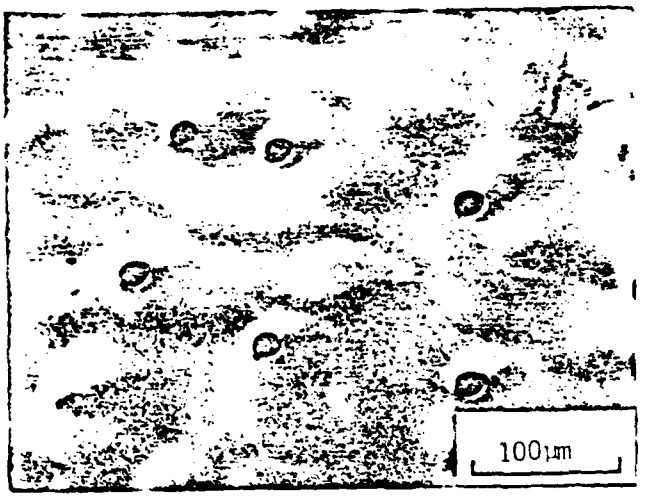


(a)



(b)

Figure 6. Surface morphology and cleaved section of double InAs layers grown with 10A/cm^2 and 13.8A/cm^2 for 15 minutes each at 620°C. The middle layer is grown from a Zn doped melt and the top layer is grown from undoped melt. The third layer is probably due to an As and/or In out-diffusion (not a grown layer).



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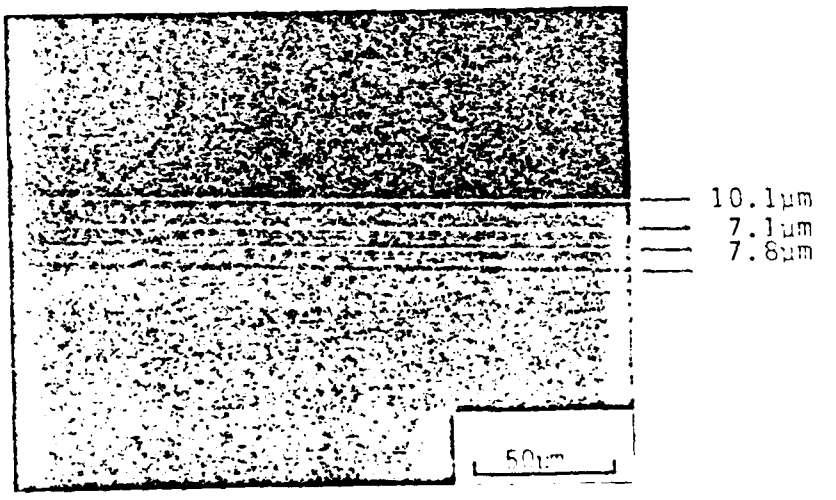

(b)

Figure 7. Surface morphology and cleaved section of double InAs layers grown with 10A/cm^2 and 13.8A/cm^2 for 15 minutes each at 620°C. The third layer is probably due to an As and/or In out-diffusion (not a grown layer).

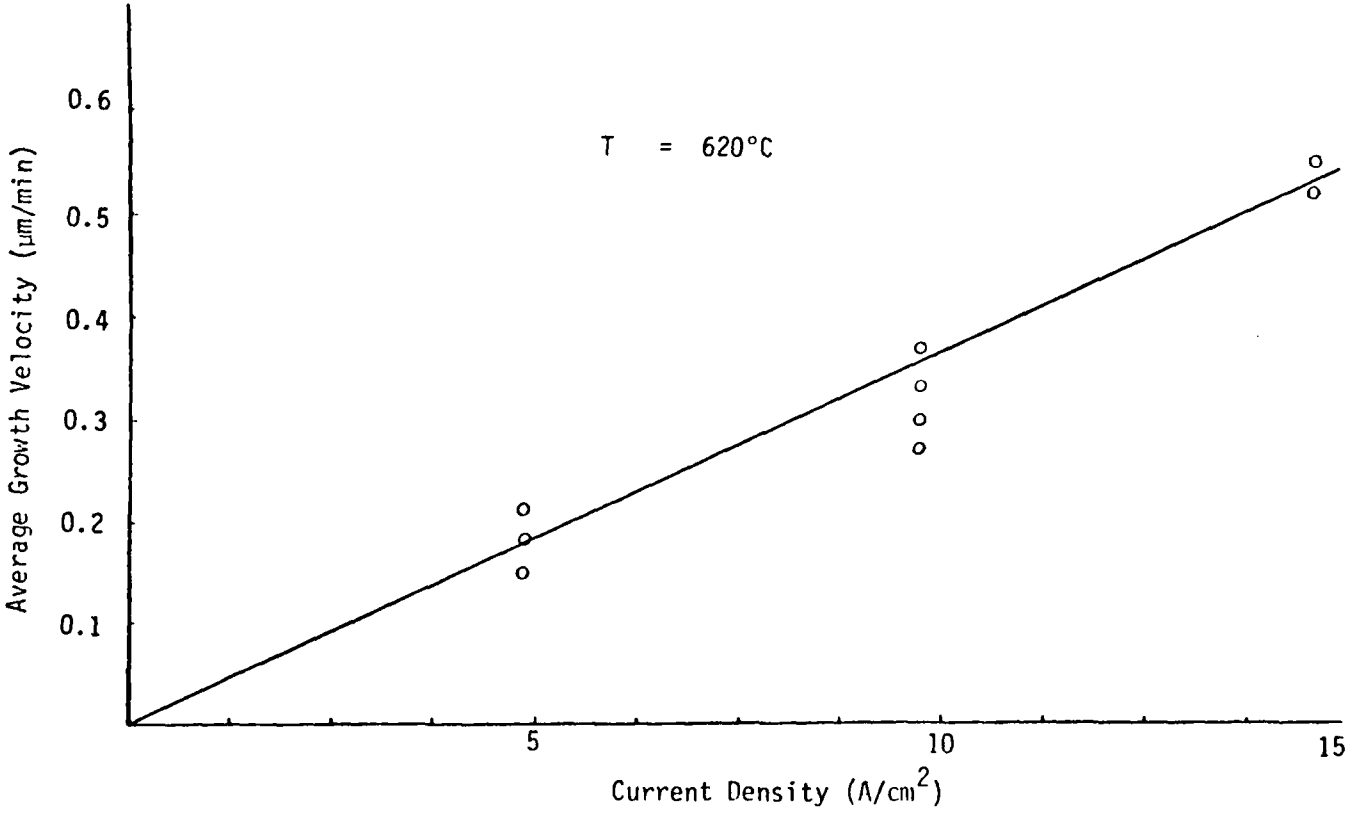

Figure 8. Average growth velocity versus electric current density for InAs grown on undoped (n-type) InAs, at 620°C.

where μ is the differential mobility of solute (As) with respect to solvent (In), E is the electric field in the melt, and C_ℓ and C_s are the concentrations of group V (As) in the melt and solid respectively.

The electric field E in the melt can be expressed in terms of the melt resistivity ρ_{In}, and the electric current density J, such as $E = \rho_{In} J$. At 620°C, $\rho_{In} = 4.33 \times 10^{-5}$ Ω-cm, $C_\ell \cong 0.058$ and $C_s = 0.5$.

Using Fig. 8 the growth velocity V for a current density $J = 10 A/cm^2$ is approximately 0.35μm/min and therefore the differential mobility can be calculated from Eq. 1 to be about $0.008\ cm^2/V\text{-sec}$.

2.2.3 Doping studies with Ge and Zn

In this work both Ge and Zn were used as dopants in InAs. Initially Ge was thought to be a p-type dopant in InAs, however, our results indicate otherwise. Layers grown from Ge doped melts showed n-type conductivity over the temperature range of 10 - 300K. Doping with Zinc (Zn) was then attempted and the results indicate that layers grown from Zn doped melts were p-type. Zinc was introduced into the melt in the form of a 7% Zn-In alloy. Since the distribution coefficient of Zn in InAs is relatively high (assumed to be ≅ 3) and the vapor pressure of Zn is high as well, the Zn in the melt has to be replenished if one were to grow several layers from the melt. Also if one desired to grow a n-type layer on the Zn doped layer one must heavily dope the second melt with n-type dopants (i.e., Ge, Te) in order to compensate for nonintentional p-doping of the second melt, as a result of the high vapor pressure of Zn.

2.2.4 Electrical Characterization of Grown Materials

Hall measurements on the grown epilayers were taken at room temperature and at 50 K temperature increments down to 10 K. Five point contacts to the sample were used to facilitate biasing of the grown layer with respect to the conducting substrate. Figures 9 and 10 show the results of Hall coefficient R_H, and Hall mobility, μ_H, versus inverse temperature performed on a p-type (Zn-doped) layer grown on a n-type substrate. Hall mobility of 2500cm^2/V-sec was obtained at about 40K and as the temperature increased the mobility decreased to about 10 cm^2/V-sec at 260 K. At temperatures higher than 260 K the Hall coefficient changed sign and the mobility increased substantially, from a low 10 cm^2/V-sec to about 10,000cm^2/V-sec at room temperature. The change in the Hall coefficient sign from + to - can be qualitatively explained using the equation

$$R_H = \frac{r_R}{e} \frac{p - b^2 n}{(p + bn)^2} \qquad (2)$$

where r_R is determined by the scattering mechanisms and is of the order of 1, e is the electronic charge, $b = \mu_n / \mu_p$ the ratio of electron to the hole mobility and p and n are the concentration of the p-type and n-type charge carriers. From Eq. (2) R_H remains positive as long as the p charge carrier exceeds $b^2 n$. As $b^2 n$ becomes close to p, R_H goes through minimum (i.e., $R_H = 0$ for $b^2 n = p$), and then changes sign to negative for $b^2 n$ greater than p. Similar behavior is expected from the Hall mobility versus inverse temperature because μ_H is the product of the Hall coefficient and conductivity, $|R_H|\sigma$.

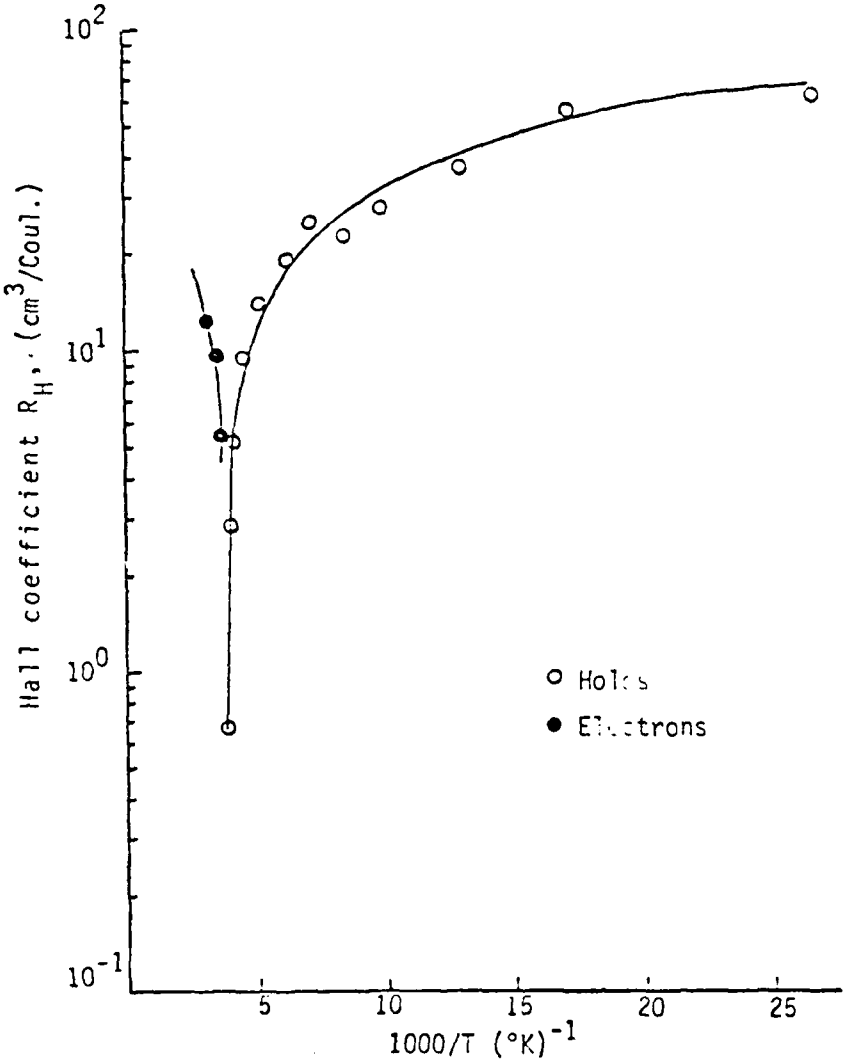

Figure 9. Hall coefficient versus inverse temperature for a p-type (Zn-doped) layer grown by CCLPE on n-type substrate (under zero bias condition).

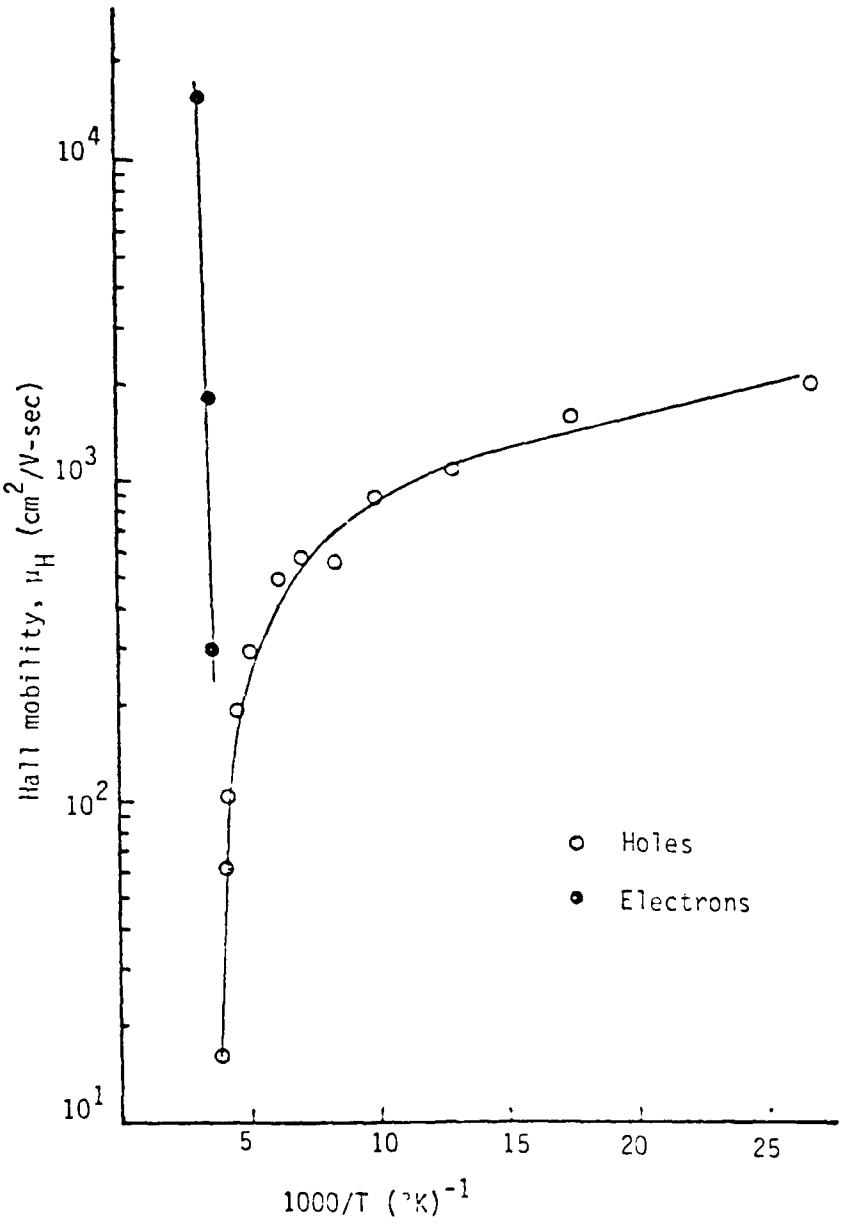

Figure 10. Hall mobility versus inverse temperature for a p-type (Zn-doped) layer grown by CCLPE on n-type substrate (under zero bias condition).

2.2.5 Temperature dependence of the I-V characteristics

In addition to the Hall measurement, I-V measurements were simultaneously made on the p-n structure over the temperature range of 10 - 300 K. Figure 11a b, c and d are photographs of the I-V characteristics of the p-n junction at 300, 150, 77 and 10 K respectively. The p-n junction seems to be very leaky at room temperature as shown in Fig. 10a and as the temperature is lowered, the reverse saturation current is decreased while the diode forward voltage is increased from less than 50mV at room temperature to about 440mV at 10 K. This behavior can be explained by the diode equation

$$I = I_o[\exp(V/V_T) - 1 \tag{3}$$

where I_o is the reverse saturation current, V is the diode voltage and $V_T = \frac{kT}{e}$ is the thermal voltage. The temperature effect on the reverse saturation current I_o, is proportional to the square of the intrinsic carrier concentration, n_i^2, as I_o, is proportional to the square of the intrinsic carrier concentration, n_i^2, as

$$n_i^2 = kT^3 \exp(-E_{g0}/kT). \tag{4}$$

From the temperature dependence of n_i^2 we obtain

$$I_o \propto n_i^2 = kT^3 \exp(-E_{g0}/kT) \tag{5}$$

Therefore, as T is lowered I_o drops fast and it moves toward the horizontal axis (i.e., toward $I_o = 0$ line). On the other hand, in order to maintain the same diode current, I, the diode voltage, V in Eq. 3 has to increase and this is verified by the temperature dependence of the I-V characteristic shown in Fig. 11b, c, and d.

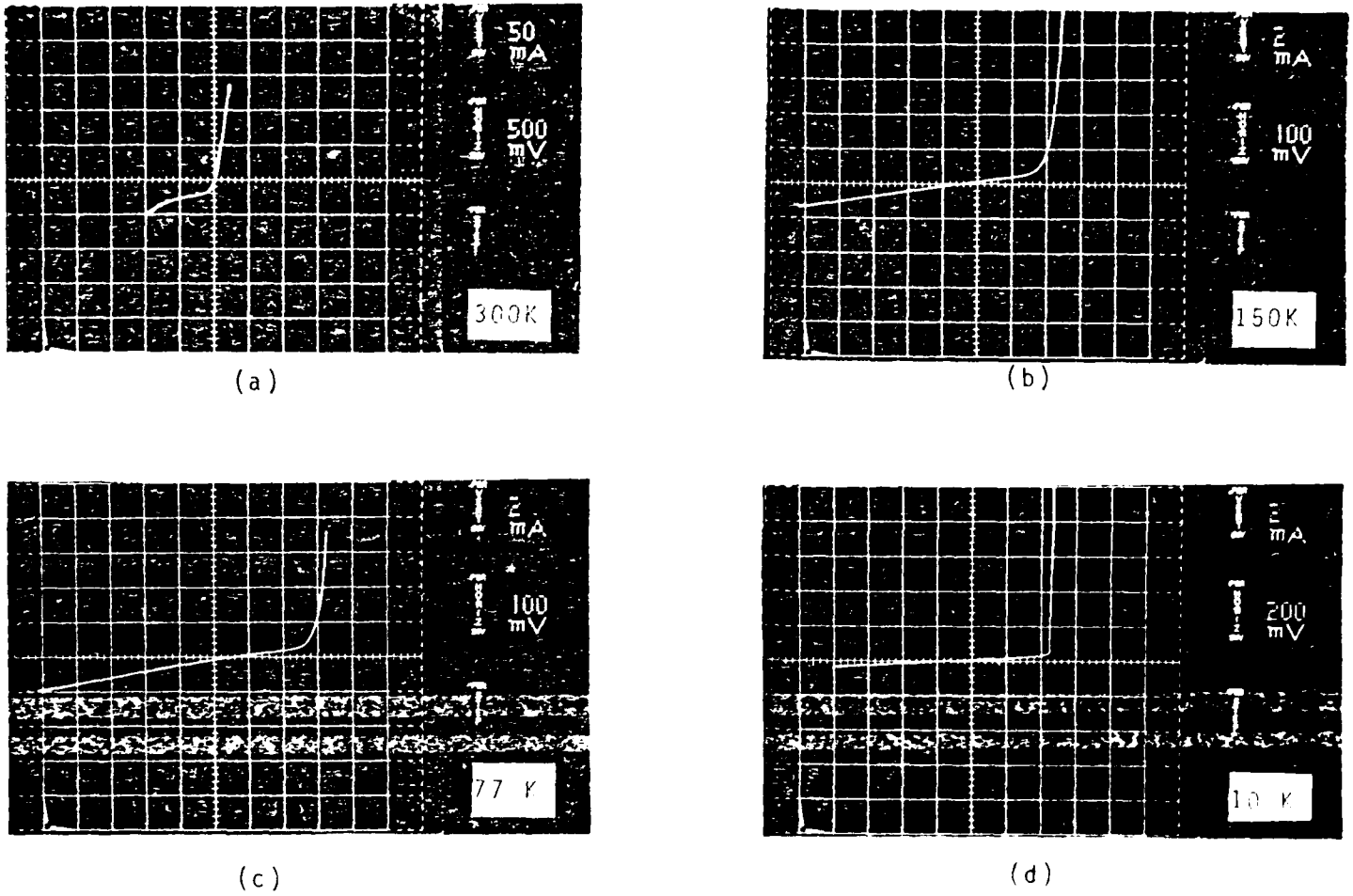

Figure 11. I-V characteristics of one layer p-n InAs vs. temperature.

2.2.6 Diffusion coefficient and differential mobility of As in In

In addition to CCLPE growth, InAs was grown by LPE in the temperature range of 570 to 670° using the CCLPE growth system shown in Fig. 12. From the LPE growth rate bersus temperature results, the diffusion coefficient of As in In was calculated to be $D = 525 \exp\left[\frac{-1.4 \times 10^4}{T}\right]$ with an activation energy for diffusion of 1.2eV or 21.8 Kcal/mole. From the CCLPE growth results, the differential mobility of As in In was computed as $\mu = 0.008\ cm^2/V\text{-sec}$ which is almost 2.5 times smaller than the differential mobility of As in Ga at the same temperature. Details of the experimental procedure and analysis of th above results are given in Appendix B.

SECTION III

3.0 GROWTH OF Si

Silicon doped with various impurities can be used as a photodetector in the infrared spectrum region. Detector-grade indium-doped silicon should have high indium concentration, good uniformity over 2-inch-or-larger wafers, and a minimum concentration of electrically active shallow defects.

3.1 CCLPE GROWTH OF Si

In this study, the current controlled LPE growth of Si was attempted by using, initially, a growth system similar to that shown in Fig. 2. and either In or Ga melts.

Generally, almost all of the growth experiments carried out were unsuccessful primarily because of the formation of a stable oxide layer on the silicon substrate and/or silicon source material at the growth temperature (850 - 1050°C). Most of the efforts were subsequently directed towards elimination or reduction of the oxide layer from the silicon surface. These efforts are described in greater detail in Appendix B and included the following; (a) Use of a three-zone Lindberg furnace and a purified argon environment to allow growths up to 1150°C. (b) Sending the graphite boat parts to POCO Graphite Co., for baking out to reduce the backgorund impurity contamination. (c) Allowing purified H_2 to pass through a mixture of Ga, In and Aℓ to further reduce the oxygen level at the inlet of the reaction tube. (d) Designing a new system such that the substrate could be kept at a cooler region during melt saturation and subsequently loaded into the boat prior to the growth run. (e) Covering the substrate

while keeping it a low temperature region in the reaction tube to prevent any deposition of impurities carried by the hydrogen stream. (f) Finally designing a completely new multiwell graphite boat, shown in Fig. 12 that would facilitate more convenient remote loading with withdrawal of the substrate.

After all of the modifications had taken place, the results indicated some improvement by achieving greater wetting on the substrate surface and some spotty growth in some experiments. The problem was always the presence of the oxide layer on the substrate surface at temperatures as low as 400°C with the oxide thickness varying from experiment to experiment. With thin oxide layers, the etchback penetrated through pinholes in the oxide and resulted in spotty growth. With thick oxide layers the etchback was completely ineffective. On the other hand, the back surface of the substrate, which was in contact with Ga at all times after loading the substrate, was completely wetted and a polycrystalline regrowth resulted as the furnace was cooled down to room temperature. This indicates that once the silicon surface is exposed to the environment in the reaction tube, it oxidizes rapidly even if the oxygen level in hydrogen is as low as 0.25 ppm, and in order to achieve wetting, the oxide (SiO_2) layer must be removed.

Considering the above results, it was decided that a more sophisticated system utilizing a controlled mixture of HF or HI, similar to the one reported by Levin[10] of RCA might be necessary to eliminate the oxide problem. However, considering the system complexity, insufficient remaining time and possible side effects in the quartz reaction tube and impurity concentration in any grown layer, it was decided to not pursue such approach.

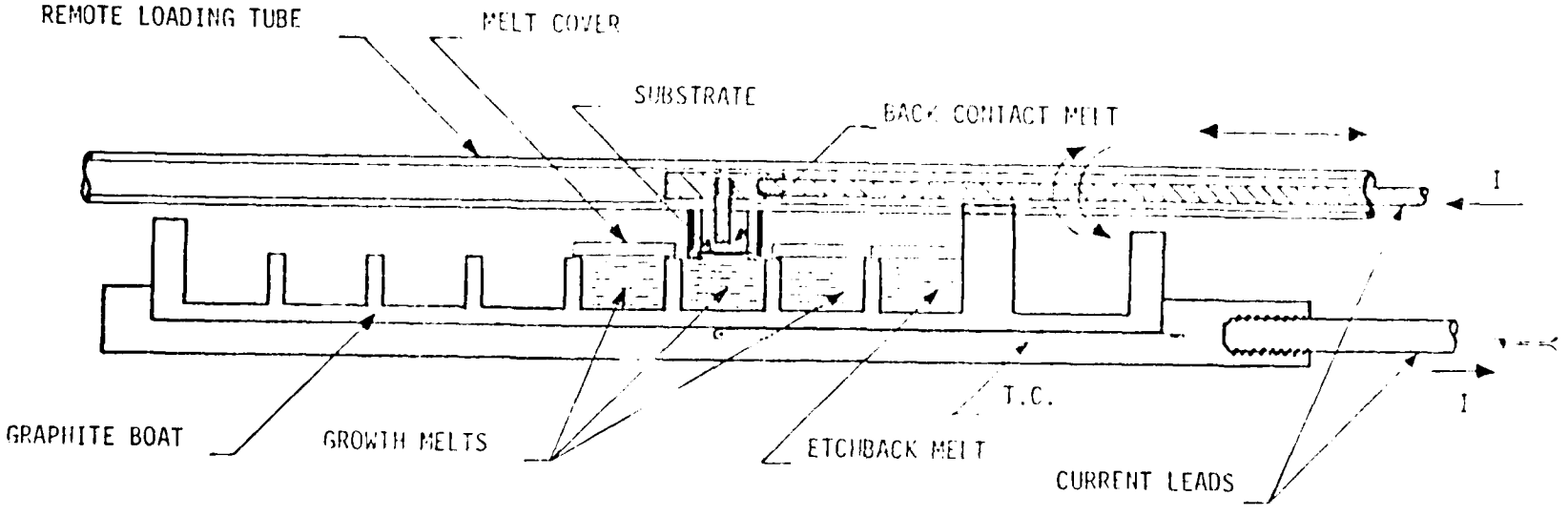

FIGURE 12. Schematic cross-section of the horizontal multiwell graphite boat for CCLPE growth.

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APPENDIX A

DIFFUSION COEFFICIENT AND DIFFERENTIAL MOBILITY OF AS in In FOR LPE AND CURRENT CONTROLLED LPE

INTRODUCTION

Current controlled liquid phase epitaxy (CCLPE) and thermal liquid phase epitaxy (LPE) are widely used techniques for the growth of III-V semiconductor compounds and alloys of high crystal quality. To analyze the experimental results and to understand the kinetics of growth of any epilayer grown by these two techniques, it is essential to have a knowledge of certain parameters, namely, solute diffusivity and solute mobility in the melt. This would enable suitable tailoring of growth parameters to achieve good quality layers for device purposes.

InP and its related alloys, $In_xGa_{1-x}As$ and $In_xGa_{1-x}As_yP_{1-y}$ lattice matched to InP, are currently of great interest due to their potential applications in microwave and optoelectronic devices. These compounds and alloys have been grown by these two LPE techniques[1-5]. Solute diffusivity[6] and mobility of P[1] are reported in literature. However, no direct or indirect measurements of these two parameters appear to have been made so far for the solute As.

We have, therefore, investigated the solute diffusivity and mobility of As by studying the LPE and CCLPE growth of InAs. In this paper, the growth rate of LPE grown InAs layers has been examined as a function of the growth parameters, namely, growth time and growth temperature. It is shown that the diffusion of the solute is the rate limiting factor for the growth rate of InAs. This feature is utilized to deduce a semiempirical expression for the variation of diffusivity of As with temperature. Furthermore, the linear relationship between the growth rate and the current density, for CCLPE grown InAs layers, allows an estimation of the differential mobility of As in In.

EXPERIMENTAL PROCEDURE

The growth method utilizes the conventional horizontal multiple well slider boat in a semitransparent furnace, as described elsewhere[3], with a small modification. The slider contains two recesses, one for the substrate and the other for the saturation substrate. Wells of dimensions 1.1 x 1.1cm and 0.7 x 0.7cm were used for LPE and CCLPE growth, respectively. Horizontal and vertical temperature gradients were maintained within a fraction of 1°C/cm in order to minimize convection currents in the melt. <100> oriented InAs substrates were used. These were chemically polished with a 0.5% bromine-methanol solution to a thickness of 300μm.

The growth melt and the substrate back-contact melt consist of accurately weighed 6N In and undoped InAs. The growth melt height is typically ∿ 0.8cm. The back-contact melt is kept slightly undersaturated. Due to the large discrepancy between the two reported values for liquidus temperatures of InAs[7,8] we redetermined the liquidus temperature by visually inspecting the melt through the semitransparent furnace. The furnace was initially raised to a temperature at which the solid InAs was completely dissolved, then the furnace temperature was lowered by ≈ 20°C, leading to partial solidification. Thereafter, the temperature was increased at a very small rate and the temperature at which the entire solid dissolved was determined as the liquidus temperature. Our results are in close agreement with Perea, et. al[7], within ± 1°C. Thus, the liquidus curve is well represented by the expression[7]:

$$X_{As}^{\ell} = 404 \exp\left(\frac{-7877}{T}\right) \qquad (1)$$

Prior to the growth run, the substrates were degreased in trichlorethylene, acetone and methanol, sequentially, and etched in 0.5% bromine-methanol solution. For CCLPE growth, to establish contact to the back of the substrate,

it is necessary to mount an additional InAs substrate at the end of the plunger which ensures the saturation of the back-contact melt and facilitates the retraction and advancement of the melt. Uniform wetting of the back surface of the substrate was achieved using this melt.

In a typical growth run, the melt is baked for ~ 5 hours at the growth temperature. Care is taken to prevent temperature overshooting during the saturation period, thus eliminating the possibility of any supersaturation during the growth cycle. To ensure that the melt is not undersaturated prior to the growth, the melt is equilibrated on the saturation substrate for a period of 1-2 hours. Next, the substrate is slid underneath the melt and the furnace is cooled linearly with time at the desired cooling rate. The CCLPE growth is accomplished by passing a dc current across the substrate-melt interface and advancing the back-contact melt to establish electrical contact.

RESULTS AND DISCUSSION

Surface Morphology

Figures 1a and 1b show typical photomicrographs of InAs layers grown by LPE and CCLPE at ~ 620°C. Figures 1c and 1d show the corresponding stained and cleaved sections. Both the LPE and CCLPE grown layers exhibit terracing. The interesting feature is that there always exists an underlying layer irrespective of the growth technique used. The thickness of this layer is found to be independent of the growth time, thus ruling out the possibility of any As diffusion from the epilayer. In order to examine whether this layer is associated with the degradation of the substrate, freshly cleaved samples of InAs were baked in the furnace at 570°C, 620°C and 660°C for a period of ≈ 7 hours in a hydrogen ambient. The samples which were baked at 570°C do not exhibit any significant change in surface topography nor the presence of any underlying layer. However, the samples baked at higher temperatures show the thermal dissociation features. This thermal dissociation may be attributed to the evaporation of arsenic, leaving an In droplet as residue on the bottom of the thermally etched pit, similar to the case of InP.[9] It is to be observed that the density and the size of the thermal pits increase with increase in baking temperature. Furthermore, the thickness of the underlying layer likewise increases with temperature. From this it may be inferred that the presence of the underlying layer is indeed associated with the thermal degradation of the substrate. However, it is not limited only to the surface layer, unlike InP samples, but also occurs beneath the surface, the depth of which depends on the baking temperature.

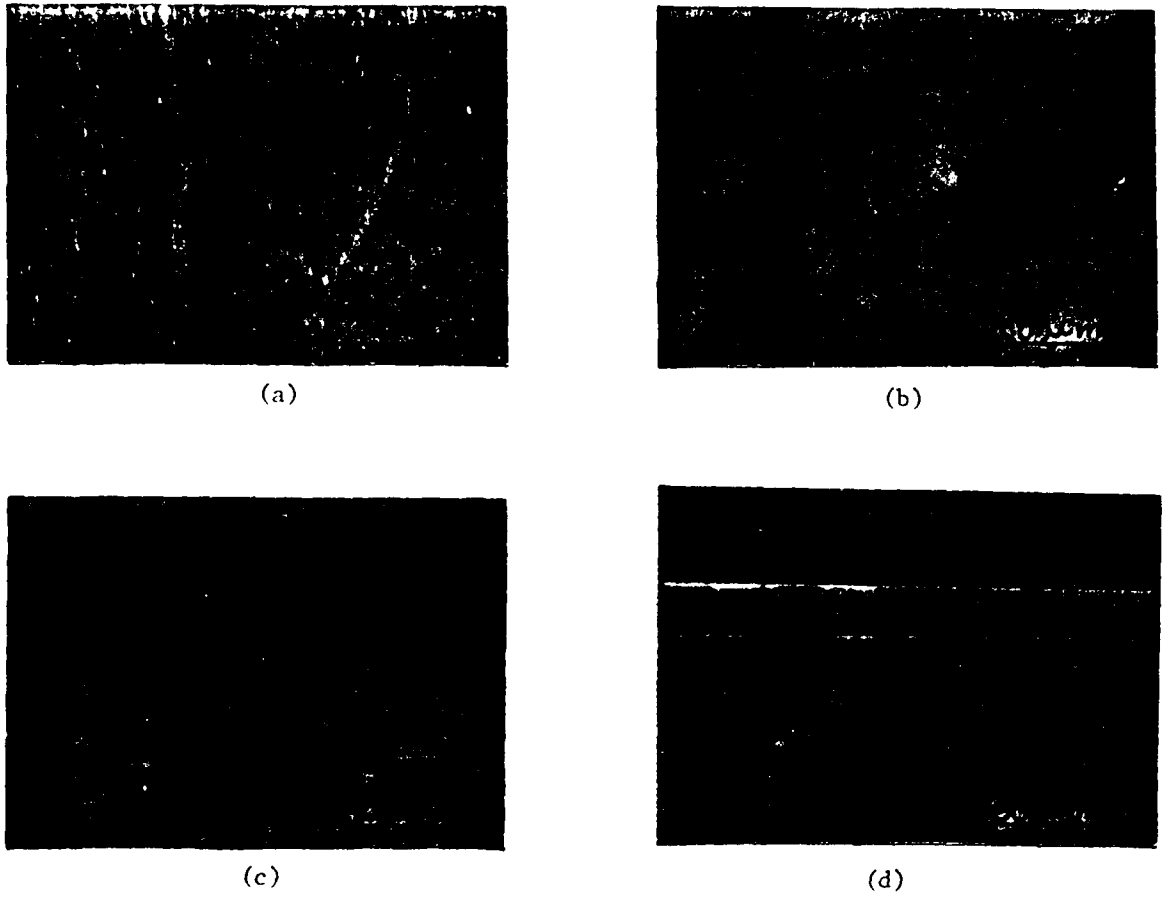

Figure 1. Nomarski phase contrast photomicrographs of surface morphology and cleaved sections of InAs layers grown by: (a) and (c) equilibrium - cooling for t = 15 min. and R = 0.27°C/min; and (b) and (d) CCLPE, two layers each grown for t = 15 min. and current density of 5 A/cm^2.

Thermal Liquid Phase Epitaxy

The simple theoretical model developed by Hsieh[6] for binary compounds grown by the equilibrium-cooling LPE technique, yields the following expression for the thickness (d) of the layer as a function of growth time (t):

$$d = \frac{4}{3} \frac{R}{C_s m} \left(\frac{D}{\pi}\right)^{\frac{1}{2}} t^{3/2} \qquad (2)$$

where R represents the cooling rate, D denotes the diffusion coefficient of the solute in the melt, m is the slope of the liquidus curve determined from Eq. (1) and C_s is the concentration of the group V element in the epilayer. If C_s and m are expressed in atomic fraction and deg/atomic fraction, respectively, then the above equation may be written as:

$$d = \frac{4}{3} \times 1.07 \frac{R}{C_s m} \left(\frac{D}{\pi}\right)^{\frac{1}{2}} t^{3/2} \qquad (3)$$

The basic assumption made in deriving this equation is that the diffusion of the solute in the melt is the rate determining step for LPE growth.

The dependence of layer thickness on the growth time is illustrated in Fig. 2 on a log-log scale. The error bar on the data point indicates the variation of thickness in the epilayer. The experiments were performed with a cooling rate of 0.27°C/min for the melt at the liquidus temperatures, T_ℓ, of 576°C and 621°C. However, for T_ℓ = 669°C, precipitates were found to float on top of the melt 3-10 minutes after the beginning of the growth. On reducing the cooling rate to 0.12°C/min no such precipitates were observed. This is attributed to the decrease in the liquidus slope with increase in growth temperature, thereby, the critical concentration, ΔC_{cr}, necessary for the spontaneous nucleation to occur is reached faster than at the lower temperature. During all the growth runs, it was ensured that the melt was

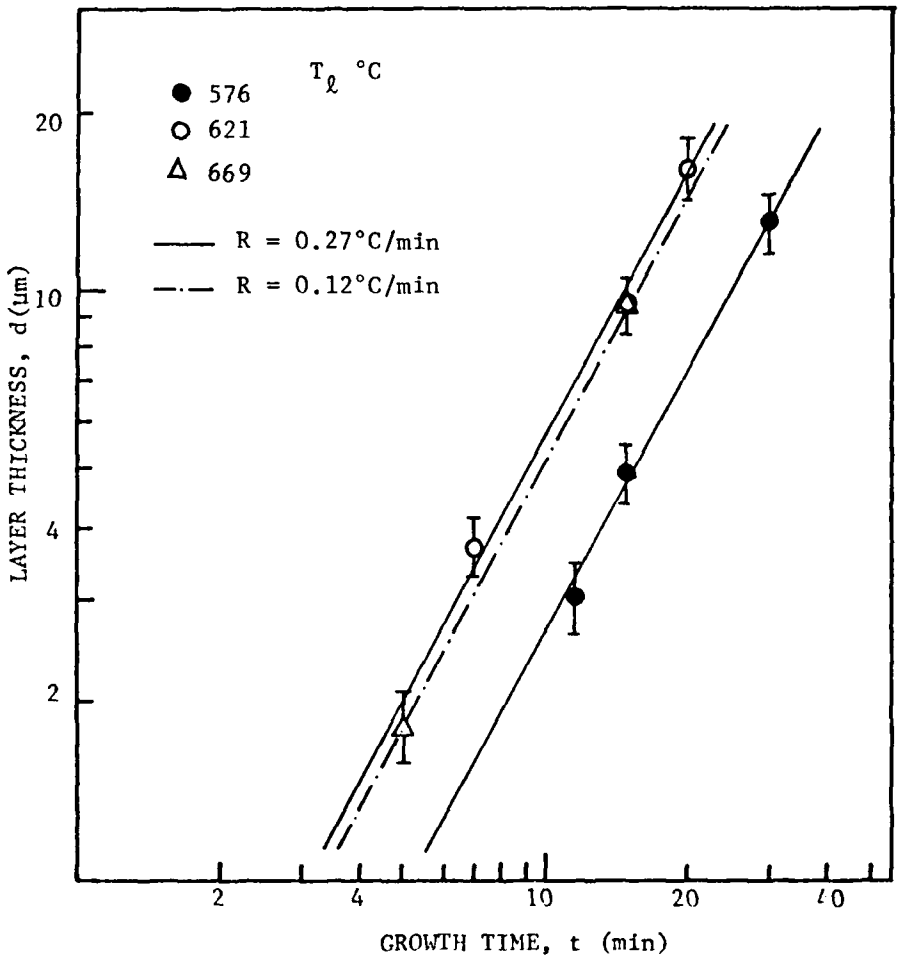

Figure 2. Variation of thickness with growth time for InAs layers from the melts of different liquidus temperatures by equilibrium-cooling.

'clean' (with no precipitation) by frequently checking the melt surface.

The linear plot of log d vs. log t as shown in Fig. 2 with a slope of 3/2 indicates that the LPE growth of InAs is diffusion limited and is consistent with the results obtained for other binary compounds[6,10,11]. Hence, with all the other parameters known, Eq(3) could be used to evaluate the diffusion coefficient. It is assumed that the liquidus slope and diffusion coefficient are invariant during the cooling interval. This is a valid assumption under the experimental conditions used, as the cooling intervals are restricted to <10°C.

Table I summarizes the data used to compute the values of the diffusion coefficient at different growth temperatures, T_m (approximately the mean temperature of the cooling intervals). The diffusion coefficient follows an exponential temperature dependence given by:

$$D = 525 \exp\left(-\frac{1.4 \times 10^4}{T}\right) \quad cm^2/sec \qquad (4)$$

and is depicted in Fig. 3. It is noteworthy that the activation energy for the diffusion process is 1.2eV, or 27.8kcal/mole, and is 1.8 times larger than the activation energy associated with the As solubility in In. A similar, but smaller increase in activation energy has been observed in GaAs[12]. However, in other binary compounds, namely InP[6] and GaP[13] the activation energy for diffusion is smaller than the activation energy associated with the solubility of the solute in the melt. This behavior of D in InAs seems to suggest strong bonding associated either between In and As or As and As.

Attempts were also made to grow LPE layers of InAs by the step-cooling technique. The main difficulty encountered was that even for a step-cooling of ~4-6°C, precipitates were formed on the surface of the melt within 5-10 minutes after the solution and substrate were brought into contact. This observation, in conjunction with an earlier result on equilibrium-cooling

TABLE I. PARAMETERS USED TO CALCULATE DIFFUSION COEFFICIENT OF As AT DIFFERENT GROWTH TEMPERATURES

GROWTH PARAMETER	LIQUIDUS TEMPERATURE, T_ℓ (°C)		
	576	621	669
T_m (°C)	573	618	668
X_{As}^m (at. frac.)	0.037	0.058	0.094
1/m (at. frac/deg)	4.02×10^{-4}	5.8×10^{-4}	8.32×10^{-4}
R (°C/min)	0.27	0.27	0.12
C_s (at. frac.)	½	½	½

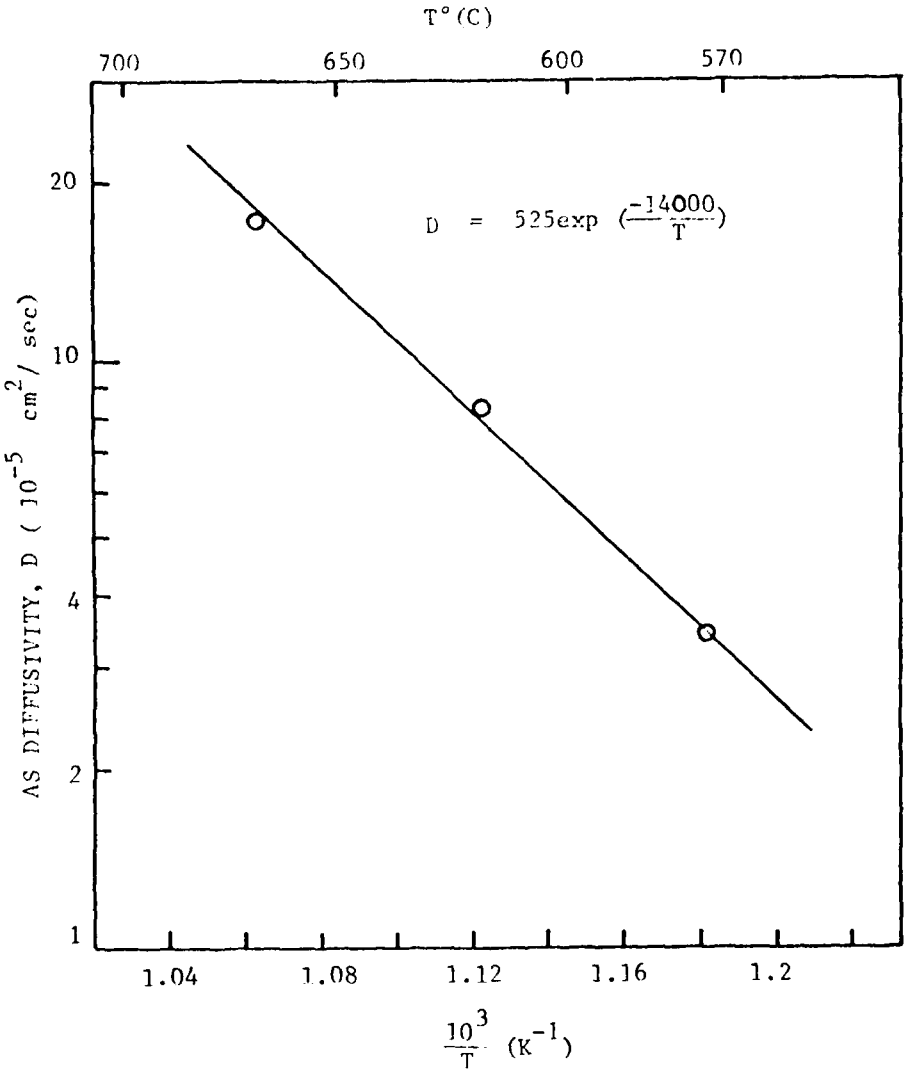

Figure 3. Temperature dependence of diffusivity of As in the In melt.

strongly suggests that the super-cooling of $\Delta T_{cr} \cong 4°C$ corresponding to a solute concentration, ΔC_{cr}, of $\sim 5 \times 10^{19}/cm^3$ is probably sufficient for spontaneous nucleation to occur. This value of ΔC_{cr} is comparable to that observed in InP[14] but less than that of GaAs[15]. Further work is needed to accurately determine the critical supercooling required for spontaneous nucleation in the InAs melt.

Current Controlled Liquid Phase Epitaxy

Figure 4 illustrates the growth rate of the epilayer as a function of current density at the substrate temperature of 620°C. Assuming electromigration to be the dominant mechanism contributing to the growth process, an analytical expression for the thickness of the epilayer is given by[16]

$$d = \mu E \left(\frac{C_\ell}{C_s - C_\ell}\right) t \qquad (5)$$

where μ is the differential mobility of the solute with respect to solvent, E is the electric field in the melt and C_ℓ is the concentration of the solute in the melt at the liquidus temperature. A least squared error analysis of the variation between the thickness of the epilayer and the growth time, as indicated in Figure 4, has been used to deduce the differential mobility of As. The average growth rate per unit current density is $\cong 0.037$ μm/min and the computed value of μ is $\cong 0.9 \times 10^{-2} cm^2/V\text{-sec}$ which is smaller than the differential mobility of As in a Ga melt[17] ($\mu \cong 2.7 \times 10^{-2}$ cm^2/sec).

CONCLUSIONS

InAs epitaxial layers have been grown by equilibrium-cooling LPE and CCLPE techniques. Thermal degradation of the InAs substrate is not limited to the surface layer but also occurs beneath the surface. The growth rate

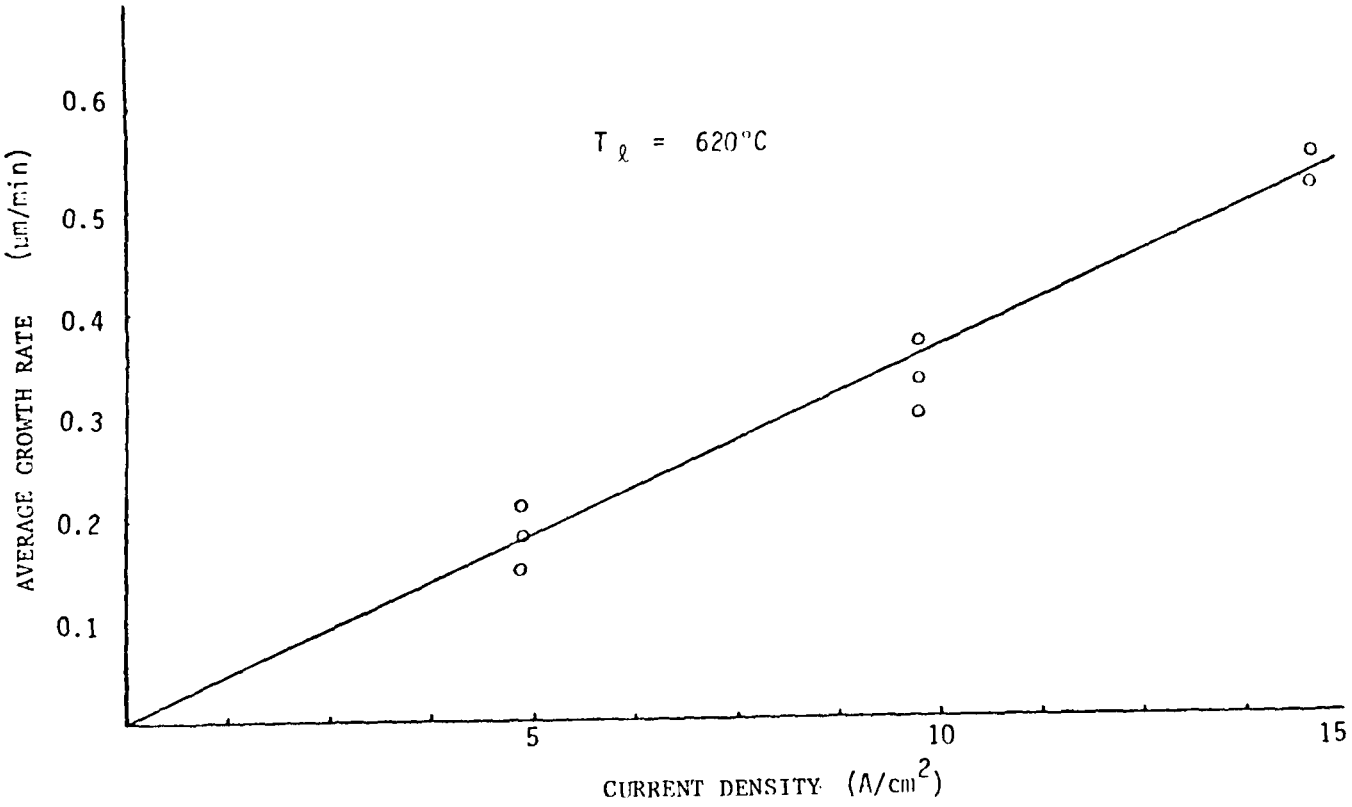

Figure 4. Average growth rate versus current density for CCLPE grown InAs layers at a constant growth temperature of 620°C.

of InAs grown by the thermal LPE technique is consistent with the diffusion limited model, and has been used to evaluate the temperature dependence of the diffusion coefficient of As. The activation energy for the diffusion process is almost 1.8 times larger than the activation energy for the solubility of As in the In melt. Solute mobility has been estimated from the linear dependence of the thickness of the grown layer on current density at the substrate-melt interface.

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APPENDIX B

CURRENT CONTROLLED LPE GROWTH OF SILICON

EXPERIMENTAL PROCEDURE AND RESULTS

To perform the growth experiments, indium (In) and gallium (Ga) were used in this study to prepare the In-Si and the Ga-Si melts. The In melt (grade A1A) 6N purity was purchased from Johnson Matthey Chemicals. A known amount of In was weighed for each of the growth melt and back contact melt and then cleaned using the following procedure: first soak twice in each of three solutions of warm tricloroethylene, warm acetone and warm methanol for 5 minutes then rinse in deionized water, then etch the In pieces of nitric acid for about 3 minutes and rinse in DI-H_2O (for slower etching hydrochloric acid is used instead). To keep the In from oxidizing, it should be rinsed and stores in isopropyl alcohol. The melts were dried with dry nitrogen and weighed again just before loading. The growth melt (about 5 grams of In) was loaded into the melt well in the boat and the back contact melt about 12 grams of In was loaded into the back contact melt well in the slider. The boat assembly was then loaded into the reaction tube. The tube was then evacuated and refilled with hydrogen twice before hydrogen is allowed to pass through the reaction tube.

The melts were then baked for 12-14 hours at a temperature of 750°C while hydrogen was flowing at approximately 100cc/min. After baking, the system was cooled down to room temperature.

Source Weight Calculation for the In-Si Melt

The solubility of silicon in In in the temperature range of 800-1100°C is reported by Thrumond and Kowalchik [1], and a reproduction of the solubility curve is shown in Figure 1. From this curve an analytical expression relating

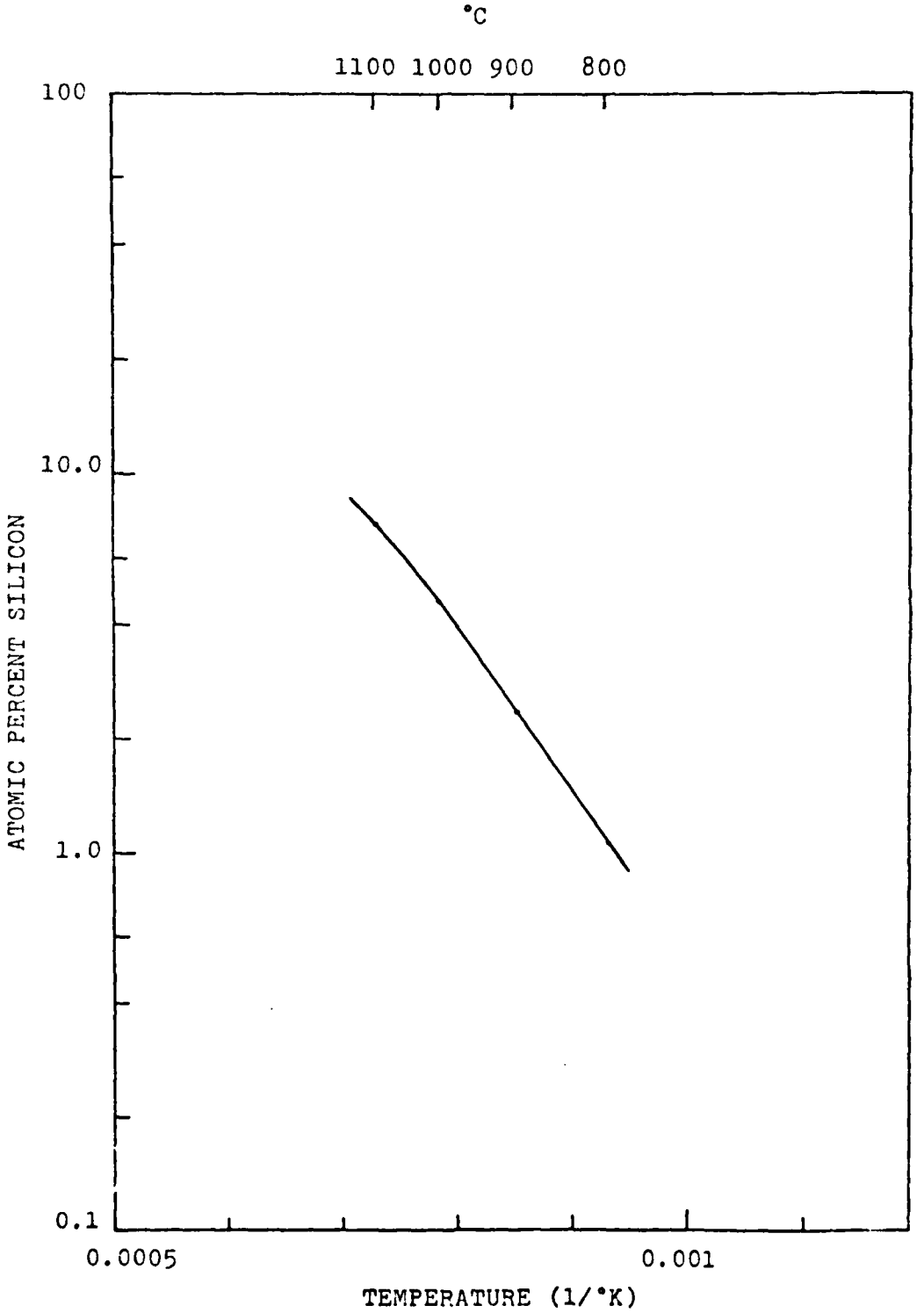

Figure 1. Silicon solubilities as a function of temperature in liquid indium. (after Thurmond and Kowalchik [1])

the atomic percent of Si to temperature in the temperature range of 900 - 1000°C is given in Eq. 1. Also using the molecular weight of In and Si Eq. 2 is derived to calculate the weight of the silicon needed for a given weight of In, as

$$X^{\ell}_{Si-In} = 1.31 \times 10^{4} \exp(-10114/T_{\ell}(k)) \quad (1)$$

Where X^{ℓ}_{Si-In} is the Atomic percent of Si in In and $T_{\ell}(k)$ is the temperature in degrees Kelvin.

$$W_{Si} = \frac{X^{\ell}_{Si-In}}{1-X^{\ell}_{Si-In}} (.245\ W_{In}) \quad (2)$$

where W_{Si} is the weight of Si corresponding to a known weight of In,

W_{In} is the weight of the In melt (grown melt or back contact melt).

Using these two equations and say a growth temperature of 900°C, it is found that about 5.8mg of silicon is needed for each gram of In.

Source Preparation

Single Crystal (111) silicon wafers were initially used for source material. An attempt to cleave one of the wafers was unsuccessful, therefore samples were cut to size by scribing the back surface of the wafer. Knowing the weight of the source needed for the growth melt and back contact melt, silicon pieces were weighed (normally 5 to 10mg more silicon was weighed in order to compensate for the silicon lost through etching), and cleaned using the following procedure: Pieces of silicon were soaked twice in each of the three solutions of tricloroethylene (TCE), acetone and methanol (5 minutes each), then rinsed twice with DI-H_2O and soaked in Hydrofloric acid for 1-2

minutes to remove any oxide layer on the surface of the silicon. This was followed with DI-H_2O rinse and then with acetic acid (CH_3COOH) rinse followed by a silicon etch which resulted in a shinny and smooth surface. The silicon etch consistes of 6HNO3:1HF:;CH_3COOH (refer to the section on silicon etchants). Etching in this solution for 5 minutes was sufficient. The etched source was then rinsed with acetic acid, DI-H_2O and isopropyl alcohol just before weighing again. Also to assure a free oxide silicon surface, a 30 second etch with Hydroflouric acid was applied, followed with DI-H_2O and isoprophyl alcohol rinses. The silicon source was then added to the baked indium. The same procedure was used to prepare the source material for the back contact melt.

Before baking the system, it was found that leaving the system purging for about 3 hours with hydrogen or Argon at small flow rates (100cc/min), to flush the air inside the tube, produced a cleaner melt after baking. Later on, when an oxygen monitor was used, it became apparent that just after loading, the oxygen content of the system is very high on the order of 10ppm which can contribute to oxidation of silicon. Flushing the system for three hours decreases the oxygen content to a few ppm.

Baking of the In-Si Melt

Heating the furnace to the saturation temperature of the InSi melt will cause the silicon to start dissolving into In. The approximate time required for the melt to saturate can be determined from the equation

$$\tau = \frac{\ell^2}{D} \qquad (3)$$

where

τ is the approximate saturation time in seconds

ℓ is the height of the Indium melt and

D is the Diffusion Coefficient of Silicon in Indium, given by [2]

$$D = 3 \times 10^{-4} \exp(-1259/T(k)) \text{ cm}^2/\text{sec.} \quad (4)$$

Therefore for a height of 5mm and a temperature of 900°C the time required for saturation is in the range of

$$\tau = \frac{.5\text{cm}}{3 \times 10^{-4} \exp\left(\frac{-1259}{1173}\right)}$$

or

$$\tau = 4.876 \times 10^3 \text{sec} \approx 1.35 \text{ hr.}$$

Practically, saturation time greater than this was required to dissolve the silicon into indium. The main reason for this was the oxide formation on the surface of the silicon source which prevented the silicon surface to wet in indium. It was therefore necessary to increase the temperature of the furnace by as much as 50°C above the saturation temperature to speed up the dissolution of Si in In. Some of the silicon was turned into oxide which floated on the top of the melt. To reduce oxidation of silicon different methods were tried with varying degree of success.

Growth Results with the In-Si Melt

Initially the high oxygen content (> 10ppm) of the reaction tube caused the exposed silicon source material to oxidize rapidly as the melt was heated to the saturation temperature. The oxidation of the source material caused non-wetting with the melt and prevented dissolution of silicon. Therefore, after loading the source material, the tube was purged for several hours with

hydrogen to remove any oxygen, especially the trapped air in the boat assembly and in the surface of the graphite, and the furnace was then turned on. Later on it was found that this led to a reduction in the oxygen content of the system from 8ppm to 3ppm and resulted in partial dissolution of silicon in the indium melt even though some of the dissolved silicon turned into oxide covering the melt. These experiments were performed at a temperature of 950°C in the semi-transparent furnace. The nature of the film appeared to be of the SiO_x type, since it would be dissolved in HF and not in either HCl, H_2SO_4 or HNO_3. The formation of the SiO_x was attributed at that time, to a reaction between the H_2 ambient and the reaction tube such as

$$2H_2 + SiO_2 \rightleftarrows Si + 2H_2O$$

where the resultant H_2O would react with the In-Si melt to form a SiO_x film. Because of these results an alternate ambient to H_2, was tried. By a modification of the gas inlet system, purified Argon (a Matheson Hydrox purifier was installed to reduce the oxygen content in the Argon gas) was incorporated into the reaction tube. Several experiments were performed in this Argon atmosphere with the source either floating on top of the melt or inserted in the middle of the melt. To help wetting and also breaking the oxide layer formed, the melt was stirred using the end of the thermocouple tube at a temperature of 950°C (the maximum achievable temperature with the semi-transparent furnace). Also another experiment was performed under 24 inches of Hg. From the results of all of these experiments it was concluded that some of the Si source was dissolved and the oxide film was not as pronounced as in the case of the previous experiments (H_2 ambient) .

In order to operate at a higher temperature (1150°C), the semitransparent furnace had to be replaced with a three zone Lindberg (200-1200°C) furnace. This was done because it was thought that at a higher temperature wetting would occur more readily. Even though initial testing of the Lindberg system resulted with a satisfactory temperature profile at a temperature of 1150°C, the chromel-alumel thermocouples used to control the furnace deteriorated rapidly. In addition, another detrimental side effect of operating at high temperatures was that after baking at 1150°C, the boron nitride part of the boat was severely deteriorated. Therefore, the slider which was made of boron nitride and graphite was replaced by a new slider made of graphite and a quartz plate as the insulator.

A square hole was cut through the quartz plate and the substrate-recess (15 mils) was made using a high speed grinder. The upper part of the boat was also machined to have larger melt wells (1.1 x 1.1cm^2). A special heat shield was also installed inside the furnace tube to minimize heat losses and to keep the end cap cooler.

With this new system 125mg of silicon dissolved in 5g of indium formed an oxide layer considerably thinner than that in previous experiments. To be certain as to whether the boron nitride part was the source of contamination, some additional experiments were performed in the boat with the quartz part at 1000°C. The results of these experiments showed that the modified system worked satisfactorily with either In or Ga-melts and about eighty percent of the silicon source was dissolved in the indium melt. The oxide layer developed on the top of the melt was negligible.

Having the Hydrox purifier to remove oxygen and water vapor from argon the exit gas was monitored and about 1-2 ppm was detected, which is high for silicon LPE. The next step was to grow epitaxial layers on silicon substrates.

Initial testing of this system showed that the melt did not wipe clean from the graphite slider and this caused melt smearing as the slider was moved to different positions.

Further investigation showed that the In melt actually wet the graphite slider and a polycrystalline layer of Si precipitated on the surface of the slider. To remove this layer, it was necessary to scrape it from the surface and as a result the use of In melt was postponed until this problem of sticking as well as the oxidation problem could be resolved. The sticking problem, however, did not take place with the Ga-Si melt. In addition the oxidation of the Ga-Si melt was considerably lower and epitaxial growth did take place at much lower temperatures.

6N-Purity Ga, purchased from Alusuisse was used for the growth and back contact melt. Normally about 5 grams of Gallium was weighed and poured in one of the melt wells in the boat and about 12 grams of Ga was used for the back contact melt. Because the gallium was in liquid form, there was no way to clean it or etch it.

Source Weight Calculation for the Gallium Melt

A reproduction of the solubility curve of Keck and Broder [3] is shown in Figure 2. The curve can be represented analytically, over the temperature range of 500-900°C, by

$$X^{\ell}_{Si-Ga} = 66 \exp\left(7800/T_{\ell}\ (K)\right) \qquad (4)$$

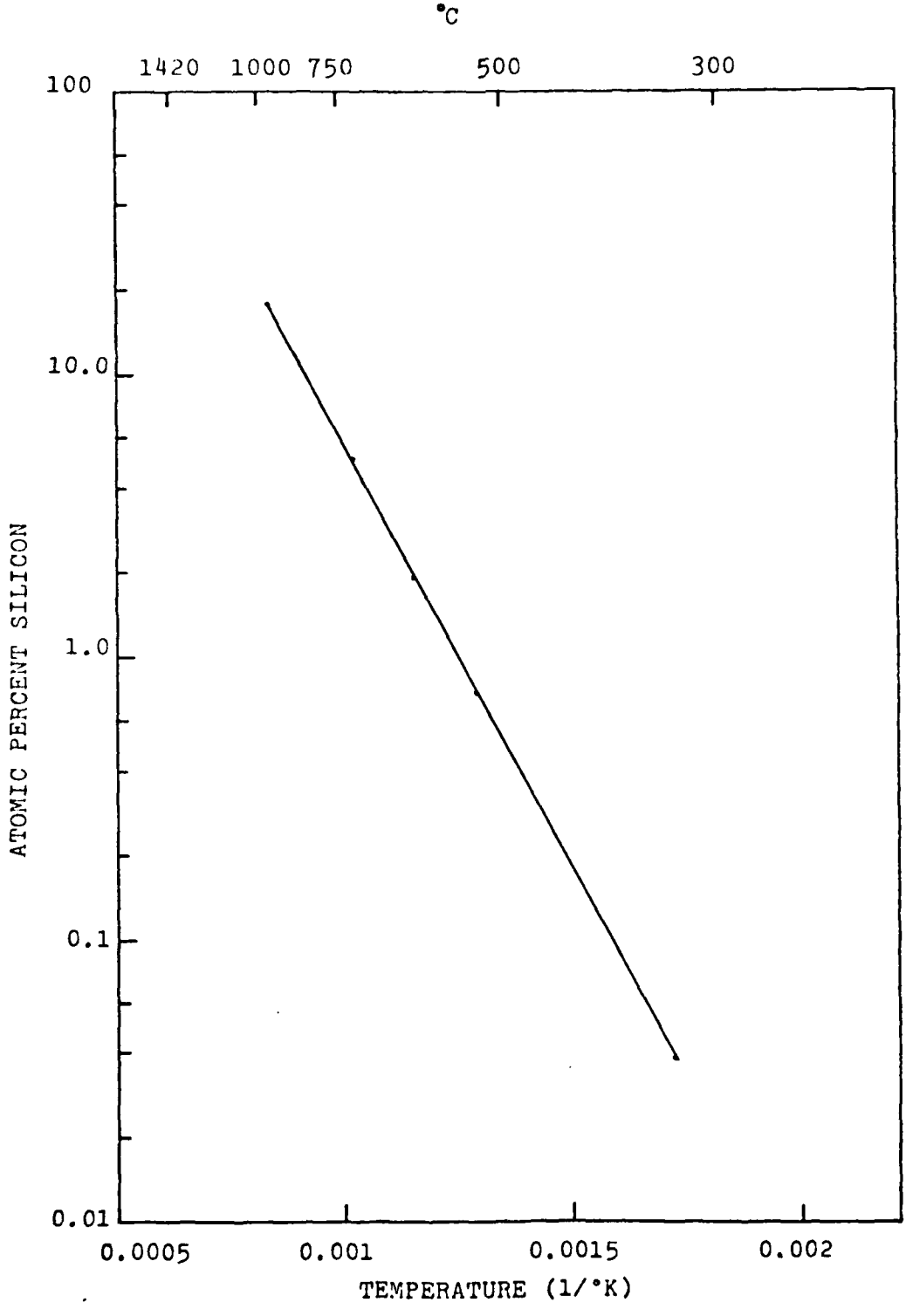

Figure 2. Silicon solubilities as a function fo temperature in liquid gallium. (after Keck and Broder [31]).

where

X^{ℓ}_{Si-Ga} is the atomic percent of silicon in Ga and $T_{\ell}(K)$ is the absolute temperature in degrees Kelvin.

Using this curve and the liquidus temperature, $T_{\ell}(K)$, the atomic percent X^{ℓ}_{Si-Ga} can be calculated. Also the weight of the silicon source needed to saturate the melt, can be found using;

$$W_{Si} = \left(\frac{X^{\ell}_{Si-Ga}}{1-X^{\ell}_{Si-Ga}} \right) \quad (.403\ W_{Ga})$$

where

W_{Si} is the weight of silicon in grams, W_{Ga} is the weight of gallium melt in grams and $_{Si-Ga}X^{\ell}$ is the liquidus atomic percent.

For example using this formula at 600°C it can be found that for each gram of gallium about 2.84mg of silicon is needed.

Baking of the Ga-Si melt

The gallium silicon melt was baked in an H_2 ambient at 800°C for about 48 hours. The minimum baking time, τ, is estimated from the diffusion coefficient of silicon in gallium, D, and the height of the melt, ℓ, such that

$$\tau_{min} = \ell^2/D$$

With $_{Si-Ga}D = 1.05 \times 10^3 \exp(-21500/T_{\ell}(K))\ cm^2/sec.$ and ℓ = 6mm, the minimum time τ_{min} is about 48 hours. The diffusion coefficient of silicon in Ga was estimated from the growth results of Sumner and Foley [4]. In actual experiments, more time was needed to dissolve the silicon source into gallium than the

calculated time. This is because of the oxidation of silicon and nonwetting with the gallium melt. Procedures similar to those developed for Si-In were used.

Substrate Preparation

Single crystal silicon wafers were cut using a wire saw to the size of 1.1 x 1.1cm^2 to be used as substrates. The wafers were mirror like polished on one side and unpolished on the other side. The substrates were cleaned using the same procedure used to clean the silicon source, followed by a Hydrofluoric acid etch for 1-2 minutes to remove any oxide on the surface. The etched substrates was then carefully placed into the substrate recess and the boat assembly was then loaded into the reaction tube. The reaction tube was evacuated to 24 inches of Hg and refilled with purified argon or hydrogen several times. This was followed by purging with the ambient gas (Ar or H_2) until the oxygen level was about 1 ppm. The furnace was then turned on and the melt was allowed to saturate at the growth temperature (600-800°C). After saturation, the growth was initiated by: a) advancing the substrate to make contact with the growth melt, (b) advancing the back contact melt to make contact with the back surface and (c) passing electric current (2-5 Amperes) across the substrate melt interface. To terminate the growth, the back contact melt was transferred to its original position, the substrate was pulled back and the furnace was turned off.

Growth Results with the Ca-Si Melt

Several growth experiments were attempted with the Ca melt at a current density of 5A/cm^2. The direction of the current flow was reversed in one of the experiments, and no current was passed while super cooling of 10°C was used in another experiment. The results of the above experiments were the same as before, that is, a few spotty areas of growth where the melt wetted

the substrate while the unwetted areas over about 95% of the surface exhibited no growth at all, even with a supercooled melt. A 5°C melt etch-back of the substrate was then attempted and after an etch back period of 30 min, a current of $5A/cm^2$ was passed across the S-M interface for 30 minutes. The net result was improved wetting of the substrate and an increase in the growth area from less than 5% of about 25%.

Several experiments were performed to grow epitaxial layers of Si on silicon substrates using the Ga-Si melt. The first melt consisted of 4.5 grams of Ga and 0.17 grams Si which was baked at 800°C for 48 hours. Using this melt for the first two experiments proved to be unsuccessful due to a short circuit in the system. The third one was a 30 minutes growth with a current of $5A/cm^2$ resulting in a few spots of growth which were not even covering one tenth of the substrate area. Using the same procedure for the fourth trial resulted in no growth at all. The reason was non-wetting of the silicon surface due to the formation of the oxide layer on the surface of the substrate and melt well. In the following two experiments, the upper melt and back contact melt were allowed to come in contact with the substrate for 15 minutes before the growth Then a 30 minute growth was carried out using a $5A/cm^2$ current, which resulted in rough layers that were covering 70% of the substrate. In the last experiment performed using the melt, in order to remove the surface oxide, through etching, the temperature of the furnace was increased by 7° while the substrate was in contact with the melt and kept there for 1 hour. Then the temperature of the furnace was decreased by 10° at a rate of 1 degree per 3 minute. The grown layer was rough again but thicker than the previous ones.

To reduce the surface oxide, another melt was prepared using a silicon chunk instead of several pieces of silicon. Experiments performed with this new melt did not yield any layer. The main reason, again, was the presence of an oxide layer on the surface of the substrate.

To make sure that no oxygen diffuses through the hydrogen gas lines, the lines were checked by a helium leak detector for any possible leaks. There was a crack found in the quartz tubing which was repaired and the oxygen level was reduced to less than 0.5 ppm. Also a Ga-Al guard melt was added surrounding the Ga-Si melt to absorb any oxygen before it could react with the Si in the melt. After trying to perform the growth it became apparent that the melt was still covered with a thin oxide layer.

To further reduce the oxygen level in the system a new bubbler containing a mixture of Ga, In and Al was installed in the H_2 line at the inlet of the reaction tube. The gettering action takes place as oxygen and aluminum react to form Al_2O_3 which floats on top of the Ga-In-Al melt. This resulted with an oxygen level of less than .25 ppm. Once again a thin layer of oxide was formed on the melt and this resulted with partial growth.

Another approach was taken to dissociate the oxide film formed round the melt during the saturation period. This was accomplished by raising the temperature of the furnace to 1200°C (maximum operating point of the Lindberg furnace) and maintained for about 30 minutes to etch away the oxide covering the melt. After the etching was completed the temperature of the furnace was lowered to the growth temperature. The experiments which were run this way resulted in a clean melt. However, a think dark brownish layer was deposited on the substrate which was found to be partially soluble in HF acid, therefore it was not just oxide.

To keep the substrate free of any deposition on it, larger pieces of Si were cut to act as a cover shield to protect the substrate. Using this method, the substrate came out clean, so did the melt (after the high temperature bake), however, no wetting occurred and this was attributed, again, to the oxidation of the substrate during the high temperature bake.

Once again a 900°C baking temperature to homogenize the melt was tried. The best result was growth with a big smooth islands of epitaxial layers which were covering 60% of the substrate. The growth took place for 35 minutes at 800°C with an etch back of 2 degrees for 15 minutes.

To prevent or at least minimize the oxidation of the substrate and to be able to bake the melt at a high temperature, at the same time, the substrate had to be kept at a low temperature region in the reaction tube and then loaded into the growth boat after the high temperature cycle was completed. This could be accomplished through remote loading of the substrate. The system modified to allow for remote loading of the substrate. A new boat design accommodated additional Ga melt for back etching of the substrate. Also a new substrate holder was built to be able to break the oxide layer which covered the melt and dip the substrate in the clean melt. The experiments done by using this system at 600°C resulted with complete wetting at the back surface while the front surface was etched severely by the Ga-Si melt.

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